AMENDMENT(S) TO THE CLAIMS

1. (currently amended) A method of regulating a target system, comprising the steps of:

providing a reference signal;

generating a plurality of digital signals defining a reference pulse train with a frequency dependent upon said reference signal;

providing a target system to be regulated, said target system having an output in the form of a plurality of digital signals defining a feedback pulse train having a frequency;

comparing said frequency of said reference pulse train with said frequency of said feedback pulse train;

generating a control signal dependent upon said comparison without regard to phase locking said feedback pulse train to said reference signal; and

providing said control signal as an input to said target system.

2. (original) The method of regulating a target system of claim 1, wherein said comparing step comprises substantially aligning a leading edge of each digital signal in said reference pulse train with a leading edge of each digital signal in said feedback pulse train.

3. (original) The method of regulating a target system of claim 2, wherein said step of generating said control signal comprises the substep of generating a proportional error pulse train including a plurality of digital signals, each said digital signal representing an error between a corresponding pair of aligned digital signals of said reference pulse train and said feedback pulse train.

4. (currently amended) A method of regulating a target system, comprising the steps of:

providing a reference signal;

generating a plurality of digital signals defining a reference pulse train with a frequency dependent upon said reference signal;

providing a target system to be regulated, said target system having an output in the form of a plurality of digital signals defining a feedback pulse train having a frequency;

comparing said frequency of said reference pulse train with said frequency of said feedback pulse train;

substantially aligning a leading edge of each digital signal in said reference pulse train with a leading edge of each digital signal in said feedback pulse train;

generating a control signal dependent upon said comparison without regard to phase locking said feedback pulse train to said reference signal, said generating step including the substeps of:

generating a proportional error pulse train including a plurality of digital signals, each said digital signal representing an error between a corresponding pair of aligned digital signals of said reference pulse train and said feedback pulse train;

counting up from zero with a first proportional clock CP1 at a frequency fP1 when said digital signals of said proportional error pulse train are in a high state;

resetting said first proportional clock CP1 to zero when said digital signals of said proportional error pulse train are in a low state;

loading a current value of said first proportional clock CP1 into a second proportional clock CP2 each time said first proportional clock CP1 transitions from a high state to a low state;

counting down from said loaded current value with said second proportional clock CP2 at a frequency fP2 until a zero value is reached; and

determining a proportional error term representing a time average of a signal which is held high while said second proportional clock CP2 is in a high state and held low while said second proportional clock CP2 is in a zero state, said control signal being dependent upon said proportional error term; and

providing said control signal as an input to said target system.

5. (original) The method of regulating a target system of claim 3, wherein said step of generating said control signal comprises the further substep of generating an error direction pulse train including a plurality of digital signals, each said digital signal representing a directionality of said error between said corresponding pair of aligned digital signals.

6. (currently amended) A method of regulating a target system, comprising the steps of:

providing a reference signal;

generating a plurality of digital signals defining a reference pulse train with a frequency dependent upon said reference signal;

providing a target system to be regulated, said target system having an output in the form of a plurality of digital signals defining a feedback pulse train having a frequency;

comparing said frequency of said reference pulse train with said frequency of said feedback pulse train, and substantially aligning a leading edge of each digital signal in said reference pulse train with a leading edge of each digital signal in said feedback pulse train;

generating a control signal dependent upon said comparison <u>without regard to phase locking said feedback pulse train to said reference signal</u>, said generating step including the

substeps of:

generating a proportional error pulse train including a plurality of digital signals, each said digital signal representing an error between a corresponding pair of aligned digital signals of said reference pulse train and said feedback pulse train;

generating an error direction pulse train including a plurality of digital signals, each said digital signal representing a directionality of said error between said corresponding pair of aligned digital signals;

counting up from zero with a first integral clock CI1 at a frequency fI1 when said digital signals of said proportional error pulse train are in a high state and said digital signals of said error direction pulse train are simultaneously in a high state;

counting down with said first integral clock CI1 at said frequency fI1 when said digital signals of said proportional error pulse train are in a high state and said digital signals of said error direction pulse train are in a low state;

maintaining said first integral clock CI1 at a current value when said digital signals of said proportional error pulse train are in a low state;

loading a current value of said first integral clock CI1 into a second integral clock CI2 each time said first integral clock CI1 transitions from a high state to a low state;

counting down from said loaded current value with said second integral clock CI2 at a frequency fI2 until a zero value is reached; and

determining an integral error term representing a time average of a signal which is held high while said second integral clock CI2 is in a high state and held low while said second integral clock CI2 is in a zero state, said control signal being

dependent upon said integral error term; and

providing said control signal as an input to said target system.

7. (currently amended) A method of regulating a target system, comprising the steps of:

providing a reference signal;

generating a plurality of digital signals defining a reference pulse train with a frequency dependent upon said reference signal;

providing a target system to be regulated, said target system having an output in the form of a plurality of digital signals defining a feedback pulse train having a frequency;

comparing said frequency of said reference pulse train with said frequency of said feedback pulse train, and substantially aligning a leading edge of each digital signal in said reference pulse train with a leading edge of each digital signal in said feedback pulse train;

generating a control signal dependent upon said comparison <u>without regard to phase locking said feedback pulse train to said reference signal</u>, said generating step including the substeps of:

generating a proportional error pulse train including a plurality of digital signals, each said digital signal representing an error between a corresponding pair of aligned digital signals of said reference pulse train and said feedback pulse train;

counting up from zero with a first derivative clock CD1 at a frequency fD1 when said digital signals of said proportional error pulse train are in a high state;

subtracting a current state of said first derivative clock CD1 from a current state of a register R each time said first derivative clock CD1 transitions from a high state to a low state;

loading said subtracted state into a second derivative clock CD2;

loading said current state of said first derivative clock CD1 into said register R;

resetting said first derivative clock CD1 to zero;

counting down with said second derivative clock CD2 at a frequency fD2 after said subtracted state is loaded therein;

maintaining said first integral clock CI1 at a current value when said digital signals of said proportional error pulse train are in a low state; and

determining a derivative error term representing a time average of a signal which is held high while said second derivative clock CD2 is in a high state and held low while said second derivative clock CD2 is in a zero state, said control signal being dependent upon said derivative error term; and

providing said control signal as an input to said target system.

8. (original) The method of regulating a target system of claim 1, wherein said frequency of said feedback pulse train varies with time.